(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 849 793 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
24.06.1998 Bulletin 1998/26

(51) Int. Cl.[6]: H01L 23/13, H01L 23/498, H01L 23/50

(21) Application number: 97122427.4

(22) Date of filing: 18.12.1997

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 18.12.1996 US 33673 P

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(54) Improvements in or relating to integrated circuit device packages

(57) An integrated circuit device package is (!) provided which incorporates one or more differential pairs (20) of signal lines coupled to an integrated circuit device. The differential pairs each include a first signal line (21) and a second signal line (22). The first signal lines are non-coplanar with the second signal lines. The first signal lines of the differential pairs may be provided in a first plane. The second signal lines of the differential pairs may be provided in a second plane different from the first plane. A first ground plane (51) is provided adjacent the first signal lines and a second ground plane (52) is provided adjacent the second signal lines. The spacing of respective signal lines provides, among other things, the capability of having a greater density of differential pairs of signal lines within the planar area of an integrated circuit device package.

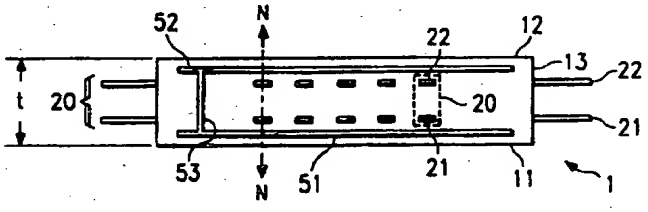

FIG. 2

EP 0 849 793 A2

Description

TECHNICAL FIELD OF THE INVENTION

This invention generally relates to integrated circuit device packages and, more particularly, to differential pair signal lines for integrated circuit device packages.

BACKGROUND OF THE INVENTION

Integrated circuit device packages are commonly arranged in a particular configuration on a printed circuit board in order to perform a desired electronic function. The integrated circuit device package may include an integrated circuit device with one or more signal lines electrically coupled to the circuitry of the device. The signal lines carry information from the device to one or more other components on the printed circuit board and carry information from the other components back to the device. This is typically known as an input/output or I/O function.

In prior integrated circuit device packages, a single, discrete signal line was dedicated to carrying information from the device to other components. A separate single transmission line was dedicated to carrying information to the device. A disadvantage of having discreet input and output signal lines is that, for a given line, noise from external sources can be introduced into the circuit by way of the signal line. In general, noise is undesirable because it degrades the signal being carried by the signal line.

One method for dealing with the problem of noise is to produce signals at a relatively high voltage (e.g., of the order of about five volts) so that the signal will be easily distinguishable from the noise. Integrated circuits are being designed, however, to operate at higher and higher speeds. Therefore, it is desirable to have a faster rise time from a state in which there is no signal to a state in which the signal exists at a functional level. The need for higher speeds and faster rise times is due in part to the increasing signal frequency at which integrated circuits are being designed to operate. One method of improving rise time is to lower the voltage value for a signal. For example, if signal voltage is of the order of about one volt, a faster rise time will be achieved than if the signal voltage is of the order of about five volts. One problem with using lower voltages, however, is that noise on the circuit is harder to distinguish from the signal being transmitted through the circuit.

A method for overcoming this problem is to use differential pairs of signal lines to achieve the input/output function. In such a system, a pair of lines is provided in which one of the lines receives information and the other line transmits information. With a differential pair, the same signal is traveling through both lines except that the polarities of the lines are opposite each other. In this configuration, the noise value on one line will cancel out the noise value on the other line of the pair, thereby achieving noise isolation.

A typical integrated circuit device package using differential pairs of signal lines is limited in the number of lines which can be incorporated into the package. A factor which limits the number of lines is the impedance characteristic of the differential pair. Impedance in an electrical circuit must be controlled and is typically set at a predetermined value. The impedance level of an integrated circuit device package and, therefore, of differential pairs within an integrated circuit device package will be dictated by the electronic device incorporating the integrated circuit device package. Impedance is generally a function of line width, line height, and separation of the lines from one another in a differential pair. Also contributing to a particular impedance is the distance from a signal line to a ground plane within the integrated circuit device package. Typical integrated circuit device packages which incorporate differential pairs of signal lines are formed such that the two signal lines which make up a given differential pair are coplanar. That is, the pair of lines exists in one plane which is parallel to the plane defined by the integrated circuit device package. Typically, a ground plane is provided in a separate plane which is different from the plane of the differential pair.

Because impedance is affected by the space between pairs and the space between the two lines of a given pair, the typical integrated circuit device package is limited in the number of differential pairs which may be provided within a given area of an integrated circuit device package. One solution is to make the lines themselves smaller, thereby allowing more pairs to coexist in a given plane. However, the capabilities within the industry in this respect are limited. Even using the smallest wires that are available in industry, it is desirable to be able to have more pairs of signal lines within a given planar area of an integrated circuit device package. Also, developing and producing smaller lines of differential pairs is costly. Further, if a line is designed to be too small, then the line might not adequately carry a signal and may become more susceptible to damage or deterioration.

SUMMARY OF THE INVENTION

It is an object of the present invention, therefore, to solve these and other shortcomings of prior integrated circuit device packages incorporating differential pairs of signal lines.

It is another object of the present invention to provide an integrated circuit device package incorporating differential pairs of signal lines in which greater numbers of differential pairs may be provided within the area of a given integrated circuit device package.

It is another object of the present invention to provide an integrated circuit device package having a greater density of differential pairs of signal lines without

substantially increasing the cost of manufacturing the integrated circuit device package.

According to a first embodiment of the present invention, an integrated circuit device package is provided which includes an integrated circuit device. At least one differential pair of signal lines is connected to the integrated circuit device. The at least one differential pair includes a first signal line, and a second signal line which is non-coplanar with the first signal line.

According to one aspect the package defines a plane. The first signal line is disposed within a first plane parallel to the plane of the package. The second signal line is disposed within a second plane parallel to the plane of the package and spaced from the first plane. According to another aspect, the first and second signal lines are disposed at different levels with respect to a thickness of the package. According to another aspect, the first and second signal lines are each intersected by a common normal of the package.

The integrated circuit device package may include a plurality of differential pairs, each having a first and a second signal line. At least one of the first signal lines is non-coplanar with at least one of the second signal lines. At least one of the first signal lines and at least one of the second signal lines may be intersected by a common normal of the package.

The integrated circuit device package may also include one or more ground planes. Preferably, the package includes at least two ground planes. A first ground plane may be provided adjacent the first signal line and a second ground plane may be provided adjacent the second signal line. The ground planes may be connected by vias.

According to a second embodiment of the present invention, an integrated circuit device package includes an integrated circuit device. The package also includes a first differential pair of signal lines electrically connected to the integrated circuit device and a second differential pair of signal lines electrically connected to the integrated circuit device. The first differential pair is non-coplanar with the second differential pair.

The first and second differential pairs may be intersected by a common normal of the package. The first differential pair may be spaced along the common normal from the second differential pair. Each of the differential pairs includes two non-coplanar signal lines.

According to a third embodiment of the present invention, a method for assembling an integrated circuit device package is provided. The method includes several steps. A first layer is formed from an encapsulation material. A second layer of a conductive material is formed over the first layer. A third layer of an encapsulation material is formed over the second layer. A fourth layer of a conductive material including a first signal line is formed over the third layer. A fifth layer of an encapsulation material is formed over the fourth layer. A sixth layer of a conductive material and including a second signal line is formed over the fifth layer.

A seventh layer of an encapsulation material may be formed over the sixth layer. An eighth layer of a conductive material may be formed on the seventh layer. A ninth layer of an encapsulation material may be formed on the eighth layer. The first and second signal lines may be intersected by a common normal of the package.

A technical advantage of the present invention is that it increases the number of differential pairs of signal lines which may be provided within a given planar area as compared to prior integrated circuit device packages.

Another technical advantage of the present invention is that greater numbers of differential pairs of signal lines may be provided in an integrated circuit device package without decreasing the size of the signal lines.

Another technical advantage of the present invention is improved electrical isolation from cross talk noise between signal pairs.

Other aspects, features and technical advantages of the present invention will be readily apparent to those having ordinary skill in the relevant art.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and for advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, wherein like reference numerals represent like parts, in which:

FIGURE 1 is a planar view of an integrated circuit device package in accordance with a first embodiment of the present invention;

FIGURE 2 is a cross-section of the integrated circuit device package of FIGURE 1 taken along lines 2-2 in FIGURE 1;

FIGURE 3 is a cross section of an integrated circuit device package in accordance with an alternative feature of the first embodiment of the present invention;

FIGURE 4 is a cross section of an integrated circuit device package according to a second embodiment of the present invention; and

FIGURE 5 shows a ball grid array package.

DETAILED DESCRIPTION OF THE INVENTION

In general, the present invention provides a differential pair geometry for allowing greater numbers of differential pairs of input/output signal lines to be provided within a given area of an integrated circuit device package. The two lines in each of the pairs are offset from each other and are disposed in separate planes as opposed to being coplanar.

As shown in FIGURE 1, a device package 1 comprises a device 10 having at least one differential pair 20 of signal lines electrically coupled to device 10 and extending therefrom. Preferably, a plurality of differential

pairs 20 of signal lines is incorporated into package 1. The device 10 and a portion of the signal lines may be encapsulated in a dielectric 30. The device 10 may be any typical integrated circuit device which can perform any desired electrical function. Preferably, device 10 is of a type suitable for high speed performance. The signal lines are provided in differential pairs 20 to provide an input/output function for device 10 relative to other components (not shown) which are electrically coupled to package 1. Device 10 and the other components may be disposed for example, on a printer circuit board (not shown). Dielectric 30 may comprise any suitable dielectric such as polyimide, FR4™, BT™ resins or a ceramic.

This arrangement may be used wherever differential pairs of signal lines are provided. This includes, for example, use with wire bonded or flip-device-type integrated circuit device packages. Also, the differential pair geometry may be used in conjunction with any type of mounting arrangement relating to the mounting of the integrated circuit device package to a printed circuit board. This includes, for example, ball grid array, pin grid array, or surface mounted peripheral packages.

As seen in FIGURE 2, each differential pair 20 includes at least one first signal line 21 and at least one second signal line 22. The signal lines of differential pairs 20 may comprise copper or any other conductive metal. Thus, a plurality of first signal lines 21 and a plurality of second signal lines 22 are preferably provided. The signal lines may be electrically connected to device 10, for example, at bond pads (not shown) of device 10.

Although the package 1 has a thickness (e.g., as designated by dimension "t" in FIGURE 2), package 10 may be viewed as defining a plane. For example, package 1 has a first side surface 11 and a second side surface 12 which are connected to each other by a perimeter surface 13. Preferably, the first and second side surfaces 11 and 12 are planar and parallel to the plane defined by the package 1. The planar area of the package is the area of either first or second side surface 11 or 12.

Each of the first signal lines 21 is preferably disposed in a first plane and each of the second signal lines 22 is disposed in a second plane different from the first plane. The first and second planes are preferably parallel to each other and to the plane of the integrated circuit device package. Therefore, the first and second planes are each parallel to the first and second side surfaces 11 and 12.

Preferably, for each differential pair 20, the first and second signal lines 21 and 22 are both intersected by a common normal to the package 1. For example, as shown in FIGURE 2, the first and second lines of a differential pair are shown being intersected by a normal N-N of package 1.

A first ground plane 51 is provided adjacent the first signal lines 21 and a second ground plane 52 is provided adjacent the second signal lines 22. Preferably, first ground plane 51 and second ground plane 52 are

coupled to each other by way of one or more vias 53 but are isolated from the respective signal lines of the differential pairs 20. Preferably, vias are provided in package 1 to interconnect first and second ground planes 51 and 52. Optionally, first and second ground plains 51 and 52 may jointly terminate, for example, at the bond pads of the device 10. Preferably, first signal lines 21 are disposed between first ground plane 51 and second signal lines 22. Preferably, second signal lines 22 are disposed between first signal lines 21 and second ground plane 52. Ground planes 51 and 52 provide a ground, carry a ground current to the device 10 and establish system impedance (together with other factors such as line width and separation).

The first lines 21 do not necessarily each have to be disposed within a single plane. Similarly, the second lines 22 do not have to be disposed in the same plane. Greater numbers of differential pairs 20 can be provided within the planar area of the package 1 as long as the first lines 21 are not coplanar with the second lines 22. For example, as shown in FIGURE 3, for a given differential pair the first line 21 is located at a first level within the thickness of the integrated circuit device package and the second line 22 is located at a second level different from the first level. However, all of the first lines 21 are not in a single plane and all of the second lines 22 are likewise not in a single plane. Preferably, for each differential pair 20, the first and second lines are still intersected by a common normal (e.g., N-N in FIGURE 3) of the package 1.

As shown in FIGURE 4, an integrated circuit device package 100 is provided which includes two layers of the type discussed above in connection with FIGURES 1-3. Integrated circuit device package 100 has differential pairs of signal lines 120 extending therefrom. In a first layer 111, the differential pairs include first signal lines 121 and second signal lines 122. A first ground plane 151 is disposed adjacent first signal lines 121 and a second ground plane 152 is provided adjacent second signal lines 122. Preferably, first signal lines 121 are disposed between first ground plane 151 and second signal lines 122. First and second ground planes may be connected by way of one or more vias 155.

In a second layer 112, the differential pairs 120 include third signal lines 123 and fourth signal lines 124. A third ground plane 153 is disposed adjacent third signal lines 123 and a fourth ground plane 154 is disposed adjacent fourth signal lines 124. Preferably, third signal lines 123 are disposed between third ground plane 153 and fourth signal lines 124. Preferably, fourth signal lines 124 are disposed between third signal lines 123 and fourth ground plane 154. Third and fourth ground planes 153 and 154 may be connected by one or more vias 156.

The signal lines 121, 122, 123, 124 are electrically connected at one end to a device (not shown) as with the previous embodiment. These components are preferably encapsulated in a dielectric 130. Second, and

third ground planes 152 and 153 may be electrically connected to each other by way of one or more vias 160. Other layers may be stacked in the manner of layers 111 and 112. According to another aspect, the integrated circuit device package 100 may also be reconfigured so that the ground planes existing between respective layers, for example, ground planes 152 and 153 are replaced with a single ground plane. As with the previous embodiment, the ground planes may comprise the same material as the signal lines (e.g., copper) or some other conductive material different from that used for the signal lines.

As shown in FIGURE 5, a ball grid array package includes at least one differential pair of non-coplanar signal lines. A differential pair of signal lines comprises first and second signal lines 221 and 222, which are oriented as described above. The lines are intersected by a common normal of the package as opposed to being in a side-by-side configuration. In other words, each line of the pair is provided in separate planes. Preferably, the planes of the signal lines are parallel to each other and to a plane defined by the package. Device 210 is provided and spaced laterally apart from the signal lines. First and second ground planes 251 and 252 are provided in a manner similar to the previous embodiments and are interconnected by vias 253. Vias 254 interconnect the first and second signal lines 221 and 222 to solder ball connectors 260, which may be used to connect the package to a printed circuit board (not shown), for example.

A first layer is formed which comprises an encapsulation material which may serve as a substrate dielectric. This layer protects the inner components of the package. A second layer is provided on the first layer. The second layer comprises a layer of conductive material which serves as the first ground plane. A third layer is provided on the second layer. The third layer comprises the encapsulation material and isolates the first ground plane from the first signal lines. A fourth layer is provided on the third layer and comprises another layer of conductive material. Portions of the fourth layer may be removed to leave the first signal lines of the respective differential pairs of signal lines. A fifth layer is provided on the fourth layer and comprises the encapsulation material. This layer isolates the first signal lines from the second signal lines. A sixth layer is provided on the fifth layer. The sixth layer comprises a conductive material, of which portions may be removed to leave the second signal lines of the respective differential pairs. A seventh layer is provided on the sixth layer and comprises the encapsulation material. The seventh layer isolates the second signal lines from the second ground plane. An eighth layer is provided on the seventh layer and comprises a conductive material to serve as the second ground plane. A ninth layer is provided on the eighth layer and comprises the encapsulation material. This layer completes the encapsulation process and protects the inner components of the package from the environment. The various layers may be provided by a known deposition technique.

Although a method of assembling the integrated circuit device packages is provided as example, any typical assembly method for integrated circuit device packages may be used so long as the first signal lines are non-coplanar with the second signal lines. Another example method of assembling integrated circuit device package is to use a ceramic substrate upon which a tungsten conductor is printed. The printed ceramic substrate is then fired in a kiln to cure the tungsten conductors.

The different dimensions of the integrated circuit device package such as the space between the first signal line and the second signal line of a given pair, the space between different differential pairs, and the space between given lines and their adjacent ground planes will be dictated by the impedance set for the integrated circuit device package. This, in turn, will be determined by the circuit impedance for the overall electronic circuit incorporating the integrated circuit device package.

Although preferred embodiments of the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made therein without departing from the spirit and scope of the invention.

Claims

1. An integrated circuit device package, comprising:

an electronic device; and

at least one differential pair of signal lines connected to the integrated circuit device, the at least one differential pair including a first signal line and a second signal line, the first signal line being non-coplanar with the second signal line.

2. The package of Claim 1, wherein the package defines a package plane, the first signal line being disposed substantially within a first plane parallel to the package plane, the second signal line being disposed substantially within a second plane parallel to the package plane and spaced from the first plane.

3. The package of Claim 1 or Claim 2, wherein the first and second signal lines are disposed at different levels with respect to a thickness of the package.

4. The package of any of Claims 1 to 3, wherein the first and second signal lines are each intersected by a common normal of the package.

5. The package of any of Claims 1 to 4, wherein the first and second signal lines are substantially parallel.

6. The package of any of Claims 1 to 5, further comprising:

a first ground plane adjacent the first signal line.

7. The package of Claim 6, wherein the first signal line is disposed between the first ground plane and the second signal line.

8. The package of Claim 6 or Claim 7, further comprising:

a second ground plane disposed substantially parallel to the first ground plane and adjacent the second signal line, the second signal line being disposed between the first signal line and the second ground plane.

9. The package of Claim 8, wherein the first and second ground planes are electrically connected by one or more vias.

10. The package of any of Claims 1 to 9, wherein the at least one differential pair comprises a plurality of differential pairs each including a first and a second signal line, at least one of the first signal lines being non-coplanar with at least one of the second signal lines.

11. The package of Claim 10, wherein the first signal lines are disposed in a plane and at least one of the second signal lines is spaced from the plane.

12. The package of Claim 10, wherein the first signal lines are disposed in a first plane and the second signal lines are disposed in a second plane different from the first plane.

13. The package of any of Claims 10 to 12, wherein the at least one first signal line and the at least one second signal line are intersected by a common normal of the package.

14. An integrated circuit device package, comprising:

an electronic device;
a first differential pair of signal lines electrically connected to the integrated circuit device; and
a second differential pair of signal lines electrically connected to the device, and wherein the first differential pair are non-coplanar with the second differential pair.

15. The package of Claim 14 wherein the first and second differential pairs are intersected by a common normal of the package, and wherein the first differential pair is spaced along the common normal from the second differential pair.

16. The package of Claim 14 or Claim 15 wherein each of the first and second differential pairs includes two non-coplanar signal lines.

17. A method for assembling an integrated circuit device package, comprising the steps of:

forming a first layer comprising an encapsulation material;
forming a second layer of a conductive material over the first layer;
forming a third layer of an encapsulation material over the second layer;
forming a fourth layer comprising a first signal line over the third layer;
forming a fifth layer of an encapsulation material over the fourth layer; and
forming a sixth layer comprising a second signal line over the fifth layer.

18. The method of Claim 17 wherein the step of forming the first and second signal lines comprise forming first and second signal lines intersected by a common normal of the package.

19. The method of Claim 17 or Claim 18, further comprising the steps of:

forming a seventh layer of an encapsulation material over the sixth layer;
forming an eighth layer of a conductive material over the seventh layer; and
forming a ninth layer of an encapsulation material over the eighth layer.

20. The method of Claim 19, further comprising the step of electrically joining the second and seventh layers by way of one or more vias.

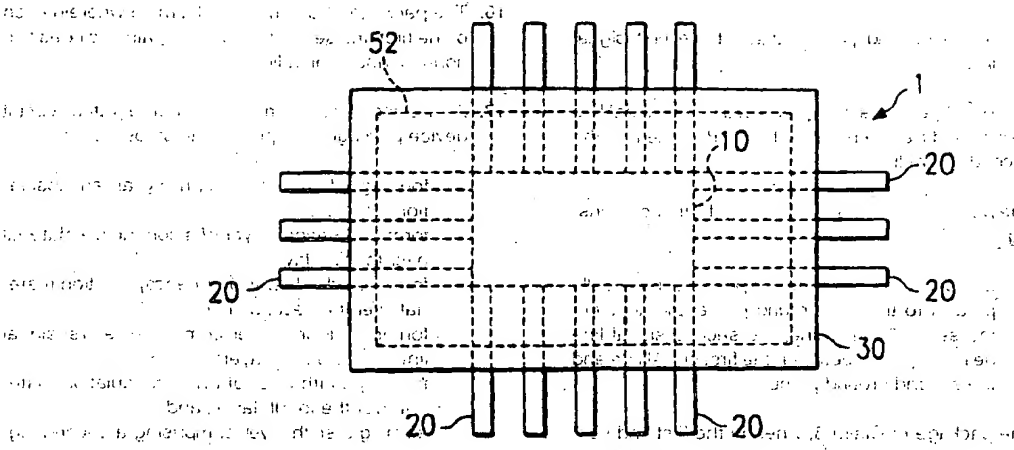

FIG. 1

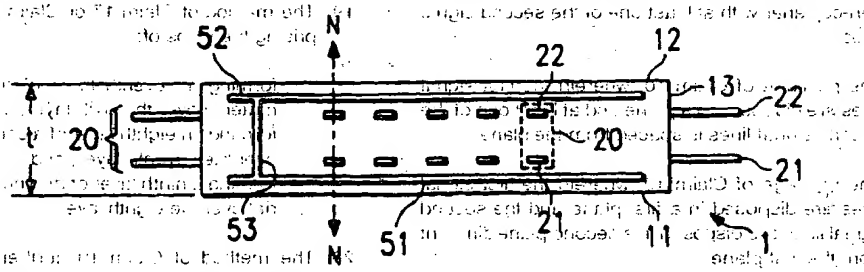

FIG. 2

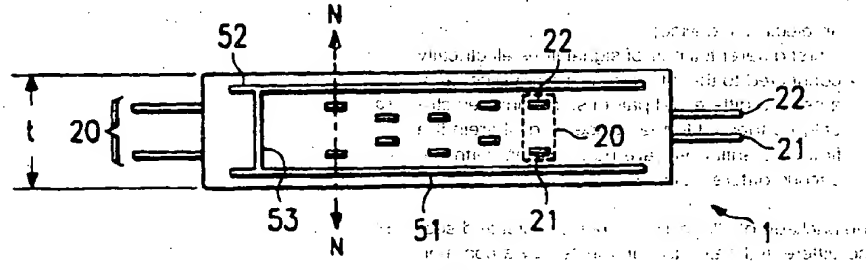

FIG. 3

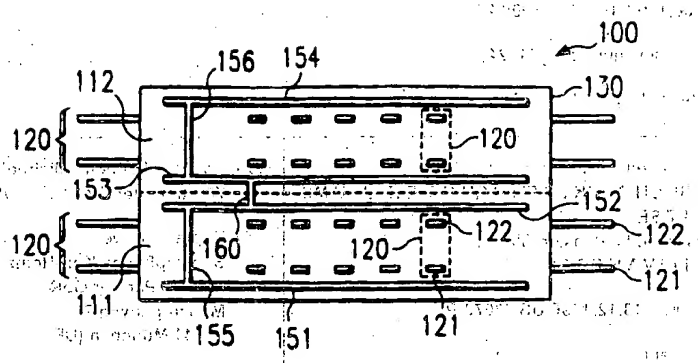
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FIG. 4

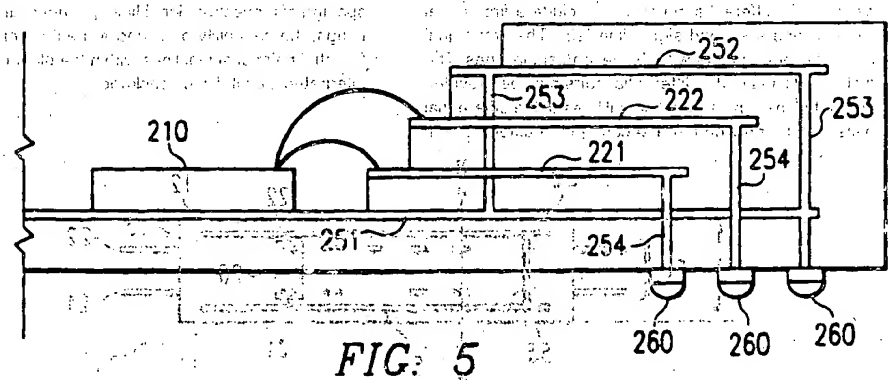
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FIG. 5

(19) Europäisches Patentamt
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(11) EP 0 849 793 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
10.05.2000 Bulletin 2000/19

(43) Date of publication A2:
24.06.1998 Bulletin 1998/26

(21) Application number: **97122427.4**

(22) Date of filing: **18.12.1997**

(51) Int. Cl.[7]: **H01L 23/13**, H01L 23/498, H01L 23/50

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **18.12.1996 US 33673 P**

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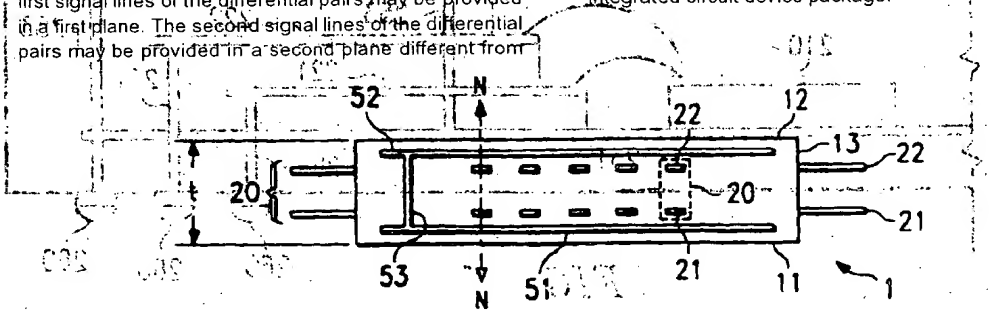

FIG. 2

EP 0 849 793 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 97 12 2427

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 499 (E-1280), 15 October 1992 (1992-10-15) & JP 04 184962 A (HITACHI LTD;OTHERS: 01), 1 July 1992 (1992-07-01) * abstract *	1-16	H01L23/13 H01L23/498 H01L23/50
A		17-20	
X	US 4 626 889 A (YAMAMOTO MASAKAZU ET AL) 2 December 1986 (1986-12-02) * column 2, line 25-51; figures 5-7 *	1-16	
A		17-19	
X	EP 0 614 331 A (IBM) 7 September 1994 (1994-09-07) * column 1, line 25-55 * * column 4, line 1-10; figures 2,3 *	1-7	
A		8-19	
X	PATENT ABSTRACTS OF JAPAN vol. 009, no. 284 (E-357), 12 November 1985 (1985-11-12) & JP 60 125002 A (NIPPON DENSHIN DENWA KOSHA), 4 July 1985 (1985-07-04) * abstract *	1-7	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A	PATENT ABSTRACTS OF JAPAN vol. 096, no. 009, 30 September 1996 (1996-09-30) & JP 08 139281 A (HITACHI LTD), 31 May 1996 (1996-05-31) * abstract *	1	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	20 March 2000	Odgers, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

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EPO FORM 1503 03.82 (P04C01)

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A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 567 (E-1296), 8 December 1992 (1992-12-08) & JP 04 218948 A (MITSUBISHI ELECTRIC CORP), 10 August 1992 (1992-08-10) * abstract *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

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THE HAGUE	20 March 2000	Odgers, M

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X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
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20-03-2000

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 04184962 A	01-07-1992	NONE	
US 4626889 A	02-12-1986	JP 1861689 C	08-08-1994
		JP 5076782 B	25-10-1993
		JP 60134440 A	17-07-1985
		DE 3446614 A	11-07-1985
EP 0614331 A	07-09-1994	US 5475606 A	12-12-1995
		DE 69401078 D	23-01-1997
		JP 6274246 A	30-09-1994
		US 5587920 A	24-12-1996
		US 5592391 A	07-01-1997
JP 60125002 A	04-07-1985	NONE	
JP 08139281 A	31-05-1996	NONE	
JP 04218948 A	10-08-1992	JP 2682727 B	26-11-1997

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82